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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/631,174	DWYER ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005 and 30 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been considered. Claims 1, 3, 4, 7, 12, 16, 20, 21, and 30 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 15 November 2004; Amendment as filed 21 March 2005; and Amendment as filed 30 June 2005.

Examiner Remarks

3. Claims 17-19 are objected to because of the following informalities: The Examiner would like to note that claims 17-19 are dependent on claim 15, whose parent independent claim is claim 12. The trend in the claims up to that point suggests that claims 17-19 should be dependent from independent claim 16 not claim 12. The Examiner has assumed for this rejection that the current claim dependencies are correct and would appreciate a confirmation or correction, if needed, regarding this matter.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-6, 12-15, 17-19, 21, and 25-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention. These claims contain the limitations, for example from claim 1, "an indicator indicative of how often a portion of said cache memory is accessed in executing said instruction from said one program" and "to store said retrieved data in said cache memory based upon said indicator." The specification lacks any description of an indicator tracking how often a portion, e.g. entry, of a cache is accessed and how this indicator is used. The specification only mentions tracking which portion has most recently been used, but not how often or the frequency a portion is accessed.

6. Claims 1-6, 12-15, 17-19, 21, and 25-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. These claims contain the limitations, for example from claim 1, "an indicator indicative of how often a portion of said cache memory is accessed in executing said instruction from said one program" and "to store said retrieved data in said cache memory based upon said indicator." A person of ordinary skill in the art would not know how to make and/or use the limitations cited above without undue experimentation, since it is not described in the specification.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-6, 12-15, 17-19, 21, and 25-29 recite the limitations, for example from claim 1 "an indicator indicative of how often a portion of said cache memory is accessed in executing said instruction from said one program" and "to store said retrieved data in said cache memory

based upon said indicator" or similar. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-11, 16, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al., U.S. Patent Number 6,587,937 (herein referred to as Jensen) in view of Burton et al., U.S. Patent Number 6,738,865 (herein referred to as Burton) and in further view of Free On-Line Dictionary of Computing's "Pipeline" ©1996 (herein referred to as FOLDOC).

11. Referring to claims 1, Jensen has taught a computer system for efficiently executing instructions of computer programs, comprising:

a. Said processing circuitry configured to stop executing said one program during a first context switch in response to a first context switch command and to resume executing said one program during a second context switch in response to a second context switch command (Jensen column 1, line 53 to column 2, line 14; column 3, lines 27-56; and column 5, lines 25-34);

b. Cache memory (Jensen column 3, lines 21-26; column 4, lines 29-37; and Figure 1);

c. Computer memory having a plurality of addresses (Jensen column 3, lines 21-26; column 4, lines 2-5; column 4, line 62 to column 5, line 13; Figure 1; and Figure 3); and

d. Memory control circuitry coupled to said processing circuitry (Jensen column 3, lines 57 to column 4, line 22; Figure 1; and Figure 2),

e. Said memory control circuitry configured to store, in response to said first context switch command, in computer memory data written during execution of said one program (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7) and

f. To store an indicator (Jensen column 6, line 65 to column 7, line 58; Figure 6; and Figure 7),

g. Said memory control circuitry, in response to said second context switch command, configured to identify one of said addresses of said computer memory that is storing said indicator corresponding to data previously written during execution of an instruction of said one computer program prior to said first context switch (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

h. Said memory control circuitry further configured to retrieve said data from said computer memory in response to said second context switch command (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11;

column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7) and to store said retrieved data in said cache memory based upon said indicator (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

12. Jensen has not taught an indicator indicative of how often a portion of said cache memory is accessed in executing said instructions from said one program. However, Jensen has taught that the state of a processor includes flags, e.g. indicators, that contain the operation status of a particular process (Jensen column 7, lines 13-29). Burton has taught an indicator indicative of how often a portion of said cache memory is accessed in executing said instructions from said one program (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1). A person of ordinary skill in the art at the time the invention was made, and as taught by Burton, would have recognized that the indicators of Burton improves cache hit ration (Burton column 2, lines 27-30), thereby increasing performance and data throughput (Burton column 1, lines 61-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the indicators of Burton in the device of Jensen to increase performance and data throughput.

13. In addition, Jensen has not taught

a. Processing circuitry having a pipeline and

b. Said pipeline configured to execute instructions from one of a plurality of programs.

14. FOLDOC has taught

a. Processing circuitry having a pipeline (FOLDOC paragraph 1) and

b. Said pipeline configured to execute instructions from one of a plurality of programs (FOLDOC paragraph 1).

15. A person of ordinary skill in the art at the time the invention was made, and as taught by FOLDOC, would have recognized that pipelining increases parallelism (FOLDOC paragraph 1), thereby providing greater throughput (FOLDOC paragraph 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of FOLDOC in the device of Jensen for greater throughput.

16. Referring to claim 2, Jensen has taught wherein said processing circuitry is further configured to execute instructions of another of said computer programs in response to said first context switch command (Jensen column 1, line 53 to column 2, line 14; column 3, lines 27-56; and column 5, lines 25-34).

17. Referring to claim 3, Jensen has taught wherein said memory control circuitry is further configured to determine, in response to said second context switch command, whether said data was utilized by said processing circuitry to execute an instruction within a specified time period prior to said first context switch (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

18. Referring to claims 4-6, Jensen has taught

a. Wherein said memory control circuitry is configured to maintain a plurality of mappings (Applicant's claim 4) (Jensen column 4, line 62 to column 5, line 13;

column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

b. Each of said mappings respectively correlating data stored in said cache memory with one of said memory addresses of said computer memory (Applicant's claim 4) (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

c. Said memory control circuitry further configured to maintain a bit of information that is associated with one of said mappings (Applicant's claim 4) (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

d. Wherein said memory control circuitry is further configured to determine, in response to said second context switch command, whether said data value was recently utilized by said processing circuitry to execute an instruction prior to said first context switch (Applicant's claim 5) (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

e. Wherein said memory control circuitry is further configured to store said mappings to said computer memory in response to said first context switch command and to retrieve said mappings from said computer memory in response to said second context switch command (Applicant's claim 6) (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

19. Jensen has not taught

a. Said memory control circuitry configured to assert said bit when a data value correlated with a computer memory address via said one mapping is utilized to execute an instruction of said one program (Applicant's claim 4), and

b. Said memory control circuitry further configured to deassert said bit periodically (Applicant's claim 4).

20. However, Jensen has taught that the state of a processor includes flags, e.g. indicators and bits, that contain the operation status of a particular process that are stored and retrieved on context switches (Jensen column 7, lines 13-29). Burton has taught

a. Said memory control circuitry configured to assert said bit when a data value correlated with a computer memory address via said one mapping is utilized to execute an instruction of said one program (Applicant's claim 4) (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1),

b. Said memory control circuitry further configured to deassert said bit periodically (Applicant's claim 4) (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1).

21. A person of ordinary skill in the art at the time the invention was made, and as taught by Burton, would have recognized that the indicators of Burton improves cache hit ration (Burton column 2, lines 27-30), thereby increasing performance and data throughput (Burton column 1, lines 61-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the

time the invention was made to incorporate the indicators of Burton in the device of Jensen to increase performance and data throughput.

22. Referring to claim 7 and 16, taking claim 7 as exemplary, Jensen has taught a computer system for efficiently executing instructions of computer programs, comprising:

a. Said processing circuitry configured to stop executing said one program during a first context switch in response to a first context switch command and to resume executing said one program during a second context switch in response to a second context switch command (Jensen column 1, line 53 to column 2, line 14; column 3, lines 27-56; and column 5, lines 25-34);

b. Cache memory (Jensen column 3, lines 21-26; column 4, lines 29-37; and Figure 1);

c. Computer memory having a plurality of addresses (Jensen column 3, lines 21-26; column 4, lines 2-5; column 4, line 62 to column 5, line 13; Figure 1; and Figure 3); and

d. Memory control circuitry coupled to said processing circuitry (Jensen column 3, lines 57 to column 4, line 22; Figure 1; and Figure 2),

e. Said memory control circuitry configured to maintain a plurality of mappings (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

f. Said mappings respectively correlating data values previously written by said pipeline during execution of an instruction and stored in said cache memory with said memory addresses of said computer memory (Jensen column 4, line 62 to

column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

g. Said memory control circuitry configured to store in said computer memory said mappings and information in response to said first context switch command and to retrieve said data values from said addresses that are identified by said mappings stored in said computer memory in response to said second context switch command based upon said information (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

h. Said memory control circuitry further configured to store in said cache memory said retrieved data values (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

23. Jensen has not taught information indicating whether said cache memory corresponding to said mappings was recently accessed. However, Jensen has taught that the state of a processor includes flags, e.g. indicators, that contain the operation status of a particular process (Jensen column 7, lines 13-29). Burton has taught information indicating whether said cache memory corresponding to said mappings was recently accessed (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1). A person of ordinary skill in the art at the time the invention was made, and as taught by Burton, would have recognized that the indicators of Burton improves cache hit ration (Burton column 2, lines 27-30), thereby increasing performance and data throughput (Burton

column 1, lines 61-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the indicators of Burton in the device of Jensen to increase performance and data throughput.

24. In addition, Jensen has not taught

a. Processing circuitry having a pipeline and

b. Said pipeline configured to execute instructions from one of a plurality of programs.

25. FOLDOC has taught

a. Processing circuitry having a pipeline (FOLDOC paragraph 1),

b. Said pipeline configured to execute instructions from one of a plurality of programs (FOLDOC paragraph 1),

26. A person of ordinary skill in the art at the time the invention was made, and as taught by FOLDOC, would have recognized that pipelining increases parallelism (FOLDOC paragraph 1), thereby providing greater throughput (FOLDOC paragraph 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of FOLDOC in the device of Jensen for greater throughput.

27. Claim 16 has similar limitations to claim 7 and is rejected for the same reasons as claim 7 above. Claim 16 differs on in that it is a method rather than a system as in claim 7.

28. Referring to claim 8, Jensen has taught wherein said processing circuitry is further configured to execute instructions of another of said computer programs in response to said first context switch command (Jensen column 1, line 53 to column 2, line 14; column 3, lines 27-56; and column 5, lines 25-34).

29. Referring to claims 9, Jensen has taught

a. Wherein said memory control circuitry is further configured to maintain utilization data indicative of which of said memory addresses are storing data values accessed within a specified time period prior to said first context switch (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7), and

b. Wherein said memory control circuitry, based on said mappings and said utilization data, is further configured to select for retrieval data values identified by one of said mappings and accessed within said specified time period (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

c. Wherein each of said retrieved data values is a data value selected by said memory control circuitry based on said utilization data (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

30. Referring to claim 10, Jensen has taught wherein said memory control circuitry is further configured to store said utilization data in. said computer memory in response to said first context switch command and to retrieve said utilization data and said mappings in response to said second context switch command (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

31. Referring to claim 11, Jensen has not taught

a. Wherein said utilization data is a plurality of bits respectively associated with said mappings,

b. Wherein said memory control circuitry, for each data value accessed by said memory control circuitry, is configured to assert the bit associated with the mapping that correlates said each data value with one of said computer memory addresses, and

c. Wherein said memory control circuitry is configured to periodically deassert each of said plurality of bits.

32. However, Jensen has taught that the state of a processor includes flags, e.g. indicators and bits, that contain the operation status of a particular process that are stored and retrieved on context switches (Jensen column 7, lines 13-29). Burton has taught

a. Wherein said utilization data is a plurality of bits respectively associated with said mappings (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1),

b. Wherein said memory control circuitry, for each data value accessed by said memory control circuitry, is configured to assert the bit associated with the mapping that correlates said each data value with one of said computer memory addresses (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1), and

c. Wherein said memory control circuitry is configured to periodically deassert each of said plurality of bits (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1).

33. A person of ordinary skill in the art at the time the invention was made, and as taught by Burton, would have recognized that the indicators of Burton improves cache hit ration (Burton column 2, lines 27-30), thereby increasing performance and data throughput (Burton column 1, lines 61-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the indicators of Burton in the device of Jensen to increase performance and data throughput.

34. Referring to claims 28 and 29, Jensen has not taught

a. Wherein said memory control circuitry is further configured to track usage frequency of cache lines in said cache memory during execution of said one program (Applicant's claim 28).

b. Wherein said memory control circuitry is configured to identify said addresses of said computer memory and to retrieve said data based upon said tracked usage frequency of said cache lines (Applicant's claim 29).

35. However, Jensen has taught that the state of a processor includes flags, e.g. indicators, that contain the operation status of a particular process (Jensen column 7, lines 13-29).

36. Burton has taught

a. Wherein said memory control circuitry is further configured to track usage frequency of cache lines in said cache memory during execution of said one

program (Applicant's claim 28) (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1).

b. Wherein said memory control circuitry is configured to identify said addresses of said computer memory and to retrieve said data based upon said tracked usage frequency of said cache lines (Applicant's claim 29) (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1).

37. A person of ordinary skill in the art at the time the invention was made, and as taught by Burton, would have recognized that the indicators of Burton improves cache hit ration (Burton column 2, lines 27-30), thereby increasing performance and data throughput (Burton column 1, lines 61-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the indicators of Burton in the device of Jensen to increase performance and data throughput.

38. Claims 12-15, 17-27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al., U.S. Patent Number 6,587,937 (herein referred to as Jensen) in view of Burton et al., U.S. Patent Number 6,738,865 (herein referred to as Burton).

39. Referring to claims 12, 21, and 30, taking 12 as exemplary, Jensen has taught a method for efficiently executing instructions of computer programs, comprising the steps of:

a. Executing a plurality of computer programs in an interleaved fashion (Jensen column 1, line 53 to column 2, line 14; column 3, lines 27-56; and column 5, lines 25-34);

b. Switching which of said computer programs is being executed in said executing step (Jensen column 1, line 53 to column 2, line 14; column 3, lines 27-56; and column 5, lines 25-34);

c. Storing, prior to said switching step at an address in computer memory a data value previously written by a pipeline to cache line in execution of an instruction corresponding to one of said computer programs in said executing step and information (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7)

d. Identifying said address in response to said switching step (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7);

e. Retrieving said data value from said address based on said identifying step and in response to said switching step based upon said information (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7);

f. Storing said retrieved data value in cache memory (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7); and

g. Retrieving said data value from said cache memory in response to said executing step (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column

6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

40. Jensen has not taught information indicative of how often said cache line is accessed during execution. However, Jensen has taught that the state of a processor includes flags, e.g. indicators, that contain the operation status of a particular process (Jensen column 7, lines 13-29). Burton has taught information indicative of how often said cache line is accessed during execution (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1). A person of ordinary skill in the art at the time the invention was made, and as taught by Burton, would have recognized that the indicators of Burton improves cache hit ration (Burton column 2, lines 27-30), thereby increasing performance and data throughput (Burton column 1, lines 61-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the indicators of Burton in the device of Jensen to increase performance and data throughput.

41. Claims 21 and 30 have similar limitations to claim 12 and is rejected for the same reasons as claim 12 above. Claim 21 differs only in that it is broader in scope than claim 12, since there are no executing and switching steps in claim 21. Claim 30 differs only in that it is a system rather than a method as in claim 12.

42. Referring to claims 13-15, Jensen has taught

a. Wherein said executing step further includes the step of executing instructions of a computer program in response to said switching step (Applicant's claim 13)

(Jensen column 1, line 53 to column 2, line 14; column 3, lines 27-56; and column 5, lines 25-34), and

b. Wherein said method further comprises the steps of:

i. Determining that said address is storing a data value previously utilized in said executing step to execute an instruction of said computer program (Applicant's claim 13) (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7);

ii. Performing said identifying step based on said determining step (Applicant's claim 13) (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7);

c. Correlating, respectively, data values stored in said cache memory with addresses of said computer memory (Applicant's claim 14) (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7);

d. Wherein said executing step further includes the step of executing instructions of a computer program in response to said switching step (Applicant's claim 15) (Jensen column 1, line 53 to column 2, line 14; column 3, lines 27-56; and column 5, lines 25-34), and

e. Wherein said method further comprises the steps of:

i. Determining, based on said bit, that said address identified in said identifying step is storing a data value previously utilized in said executing step to execute an instruction of said computer program(Applicant's claim 15) (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7); and

ii. Performing said identifying step based on said determining step (Applicant's claim 15) (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

43. Jensen has not taught

a. Asserting a bit each time a data value correlated with said address identified in said identifying step is accessed in response to said executing step (Applicant's claim 14); and

b. Periodically deasserting said bit (Applicant's claim 14).

44. However, Jensen has taught that the state of a processor includes flags, e.g. indicators and bits, that contain the operation status of a particular process that are stored and retrieved on context switches (Jensen column 7, lines 13-29). Burton has taught

a. Asserting a bit each time a data value correlated with said address identified in said identifying step is accessed in response to said executing step (Applicant's claim 14) (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1),

b. Periodically deasserting said bit (Applicant's claim 14) (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1).

45. A person of ordinary skill in the art at the time the invention was made, and as taught by Burton, would have recognized that the indicators of Burton improves cache hit ration (Burton column 2, lines 27-30), thereby increasing performance and data throughput (Burton column 1, lines 61-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the indicators of Burton in the device of Jensen to increase performance and data throughput.

46. Referring to claims 17, Jensen has taught

a. Maintaining utilization data .indicative of which of said memory addresses are storing data values accessed within a specified time period prior to said first context switch (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7), and

b. Selecting, based on said mappings and said utilization data, data values accessed within said specified time period (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

c. Wherein said retrieving step includes the step of retrieving each data value selected in said selecting step (Jensen column 4, line 62 to column 5, line 13;

column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

47. Referring to claim 18, Jensen has taught Storing said utilization data in said computer memory in response to said first context switch command; and retrieving said utilization data and said mappings in response to said second context switch command (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

48. Referring to claim 19, Jensen has not taught

a. Wherein said utilization data is a plurality of bits respectively associated with said mappings, and

b. Wherein said method further comprises the steps of:

i. Asserting each of said bits associated respectively with each of said mappings that identifies a data value accessed in response to said executing step, and

ii. Periodically deasserting each of said bits.

49. However, Jensen has taught that the state of a processor includes flags, e.g. indicators and bits, that contain the operation status of a particular process that are stored and retrieved on context switches (Jensen column 7, lines 13-29). Burton has taught

a. Wherein said utilization data is a plurality of bits respectively associated with said mappings (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1), and

b. Wherein said method further comprises the steps of:

i. Asserting each of said bits associated respectively with each of said mappings that identifies a data value accessed in response to said executing step (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1), and

ii. Periodically deasserting each of said bits (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1).

50. A person of ordinary skill in the art at the time the invention was made, and as taught by Burton, would have recognized that the indicators of Burton improves cache hit ration (Burton column 2, lines 27-30), thereby increasing performance and data throughput (Burton column 1, lines 61-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the indicators of Burton in the device of Jensen to increase performance and data throughput.

51. Referring to claims 20 and 30, taking claim 20 as exemplary, Jensen has taught a computer system for efficiently executing instructions of computer programs, comprising::

a. Computer memory (Jensen column 3, lines 21-26; column 4, lines 2-5; column 4, line 62 to column 5, line 13; Figure 1; and Figure 3);

b. A processing unit comprising cache memory and logic configured to store in said computer memory a value and a mapping associated with said value (Jensen

column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

c. Said mapping indicative of a location in said computer memory storing data previously requested or previously written by an instruction of a first process being executed by the processing unit when the processing unit context switches out the first process for processing of a second process (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

d. The logic further configured to retrieve said data, based on said value, and store said data in said cache (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7),

e. Said processing unit continuing execution of said first process with the retrieved data when the processing unit context switches out the second process and context switches in the first process (Jensen column 1, line 53 to column 2, line 14; column 3, lines 27-56; and column 5, lines 25-34).

52. Jensen has not taught a value indicative of whether a portion of said cache memory was recently accessed by said processor. However, Jensen has taught that the state of a processor includes flags, e.g. indicators and bits, that contain the operation status of a particular process (Jensen column 7, lines 13-29). Burton has taught a value indicative of whether a portion of said cache memory was recently accessed by said processor (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21;

and Figure 1). A person of ordinary skill in the art at the time the invention was made, and as taught by Burton, would have recognized that the indicators of Burton improves cache hit ration (Burton column 2, lines 27-30), thereby increasing performance and data throughput (Burton column 1, lines 61-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the indicators of Burton in the device of Jensen to increase performance and data throughput.

53. Referring to claims 22 and 25, Jensen has taught wherein said cache memory comprises a cache line (Jensen column 3, lines 21-26; column 4, lines 29-37; and Figure 1).

54. Referring to claims 23 and 26, Jensen has taught wherein said value is indicative of whether said processing unit has accessed said cache line during a particular time period (Jensen column 4, line 62 to column 5, line 13; column 5, line 52 to column 6, line 11; column 6, line 65 to column 7, line 58; Figure 3; Figure 6; and Figure 7).

55. Referring to claims 24 and 27, Jensen has not taught

a. Wherein said value indicative of said cache memory usage is defined by a flag (Applicant's claim 24),

b. Said logic configured to assert said flag when said first process uses said cache line (Applicant's claims 24 and 27).

56. However, Jensen has taught that the state of a processor includes flags, e.g. indicators and bits, that contain the operation status of a particular process (Jensen column 7, lines 13-29). Burton has taught

a. Wherein said value indicative of said cache memory usage is defined by a flag (Applicant's claim 24) (Burton Abstract; column 1, lines 40-49 and 61-63;

column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1),

b. Said logic configured to assert said flag when said first process uses said cache line (Applicant's claims 24 and 27) (Burton Abstract; column 1, lines 40-49 and 61-63; column 2, lines 3-5, 11-16, and 19-34; column 2, lines 58-66; column 3, lines 11-21; and Figure 1).

57. A person of ordinary skill in the art at the time the invention was made, and as taught by Burton, would have recognized that the indicators of Burton improves cache hit ration (Burton column 2, lines 27-30), thereby increasing performance and data throughput (Burton column 1, lines 61-63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the indicators of Burton in the device of Jensen to increase performance and data throughput.

Response to Arguments

58. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

59. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

60. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

61. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

62. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

63. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
16 September 2005

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